Next, as shown in FIG. **7**(*b*), using a mask of hotoresist or the like, a known anisotropic etching method is used to form an emitter electrode **214**, an upper electrode **215** of the capacitance and an emitter electrode outer peripheral part **218**, after which the above mask of photoresist or the like and the oxide film **210** are used as a collector trench forming mask, either etching being continued under the same etching conditions or several separated steps being performed, so as to perform etching of the first n-type well **205**, thereby forming the collector trench **216**. Next, a known method of anisotropic etching of an oxide film is used, with the exception of under the emitter electrode **214** and the upper electrode **215** of the capacitance, and the part that is left remaining as the first side wall insulation film **217** on the side wall of the aperture part of the first polysilicon **207**.

Next, as shown in FIG. **7**(*c*), a second mask **236** of photoresist or the like is used to performing etching by a known method, thereby forming the gate electrode **219**, the lower electrode **220** of the capacitance, and the ring-shaped structure **221**.

Next, as shown in FIG. **7**(*d*), the second mask **236** is removed, and a mask of photoresist or the like is used to perform ion implantation, so as to form an n-type LDD layer **222** and a p-type LDD layer **223**, and a second oxide film **224** being deposited over the entire surface to a thickness of approximately 200 nm.

Next, as shown in FIG. **8**(*a*), a known method of anisotropic etching is used to form onto the side walls of the gate electrode **219**, the emitter electrode **214**, the collector trench **216**, the upper electrode **215** of the capacitance, and the lower electrode **220** of the capacitance and the outer side wall of the ring-shaped structure **221** a side wall insulation film **225** that is formed from the second oxide film **224**.

Next, as shown in FIG. **8**(*b*), a mask of photoresist or the like is used to implant ions of phosphorus, arsenic, or the like, thereby forming an NMOS n+ type source/drain **226** and an n+ type diffusion layer **227** at the bottom of the collector trench **216***a,* after which a mask of photoresist or the like is used to perform ion implantation of boron, BF_2 or the like, thereby forming a PMOS p+ type source/drain **228** and a p+ type extrinsic base **229**.

Next, as shown in FIG. **8**(*c*), the surfaces of the gate electrode **219**, the emitter electrode **214**, the lower electrode **220** of the capacitance, the upper electrode **215** of the capacitance, the emitter electrode outer periphery part **218**, the n-type diffusion layer **227** at the bottom of the collector trench **216***a,* and n+ type source/drain **226**, the p+ type source/drain **228** and the p+ type extrinsic base **229** are silicided, thereby forming the silicide layer **130**.

Next, as shown in FIG. **8**(*d*), an interlayer insulation film **231** that is formed by an oxide film of, for example, 50 nm (TEOS-SiO_2 film) and an 800 nm BPSG film is formed, and RTA is performed for 10 seconds at 1050° C. or oven annealing is performed for 20 to 30 seconds at 900° C., thereby forming an emitter diffusion layer **232**, after which a contact hole is made and a contact plug **323** is formed on an intervening barrier metal (not shown in the drawing), after which a metal wire **234** is formed.

In experimenting with the second embodiment of the present invention, for a bipolar transistor emitter length of 20 μm (or greater, it was possible to achieve a reduction of approximately 30 to 60% in resistance that is attributed to the emitter electrode wiring resistance.

The third embodiment of the present invention is described below, with reference made to FIG. **9**. FIG. **9** is a plan view and cross-sectional view of the bipolar transistor part of a BiCMOS structure according to the present invention. In general, the parts of this embodiment that differ from the second embodiment of the present invention will be described herein.

As shown in FIG. **9**(*a*) and FIG. **9**(*b*), an emitter electrode outer periphery part **218***a* is formed so as to be connected to the ring-shaped structure **221**. The emitter electrode outer periphery part **218***a* is formed so as to have a wider wire width than in the second embodiment. The metal wire **234**E for the emitter electrode is connected to the emitter electrode via the contact plug **233** at two locations on the emitter electrode outer periphery part **218***a*. For this reason, it is possible to achieve a further decrease in the wiring resistance of the emitter electrode. In experiments with the third embodiment of the present invention, it was possible to achieve a reduction in emitter resistance of approximately 30 to 40% in comparison with the second embodiment of the present invention.

With the present inventions in a semiconductor having both a bipolar transistor and an n-channel MOS transistor and a p-channel MOS transistor on one semiconductor substrate, a gate electrode of the above-noted MOS transistor is formed by patterning of a first conductive film, the emitter electrode of the bipolar transistor is formed by patterning of a second conductive film, and also a ring-shaped structure is formed so as to surround the bipolar transistor, this being formed by patterning of the first conductive film. Another effect is that the emitter electrode outer periphery part that is electrically connected to the above-noted ring-shaped structure is formed by the patterning of the second conductive film.

Additionally, a side wall insulation film is formed from the same insulation film on the above-noted gate electrode and emitter electrode.

For this reason, not only is the construction of the BiCMOS structure simplified, but also part of the emitter electrode, that is, the emitter electrode outer periphery part about the ring-shaped structure is disposed in a ring-shaped manner, so that these elements are in mutual connection, the result being that it is possible to prevent an increase in the wiring resistance of the emitter, even with a shrinking of the feature size of the BiCMOS structure.

Additionally, the insulation film that provides insulation between the emitter electrode of the bipolar transistor and the p-type intrinsic base region and the insulation film that makes up the side wall insulation film on the CMOS transistor gate electrode side wall and bipolar transistor emitter electrode side wall insulation are different insulation films. For this reason, it possible to form a BiCMOS structure having a high reliability.

What is claimed is:

1. A semiconductor device comprising:

a bipolar transistor having an emitter electrode;

a ring-shaped conductive layer which surrounds said bipolar transistor; and

MOS transistors formed on a substrate with said bipolar transistor,

wherein side walls of gate electrodes of said MOS transistors and side walls of said emitter electrode are formed of a same insulating film.

2. The semiconductor device according to claim **1**, wherein a silicide layer is formed on the surfaces of source/drain diffusion region, and a gate electrode of said MOS transistor, said emitter electrode, and an emitter electrode outer periphery part formed on said ring-shaped conductive layer, and said emitter electrode outer periphery part on said ring shaped conductive layer is connected to said emitter electrode.